AMENDMENTS

IN THE SPECIFICATION

1) page 3, last paragraph, please replace this paragraph with the following:

For advanced FET devices, which have a channel length of 0.25 μm or less, it is difficult for the conventional process of salicidation to simultaneously meet the requirements of ultra shallow junction depth and of low sheet resistivity of the surface of the contact regions. Junction leakage can be reduced by reducing the thickness of the layer of silicide, this however increases the sheet resistivity. The invention provides a method that addresses these concerns.

2) page 4, third paragraph, please replace this paragraph with the following:

A principle objective of the invention is to provide a method of salicidation whereby uniform polishing of the salicided surfaces is maintained.

3) page 4, last paragraph, please replace this paragraph with the following:

Yet another objective of the invention is to provide a method of salicidation whereby polishing of the salicided surface can be performed using relatively relaxed parameters of polishing time, that is providing a relatively wide "processing window" for the polishing operation.

4) page 15, second paragraph, please replace this paragraph with the following:

The metal contacts with the source/drain regions and the gate electrode are formed as a final step. A dielectric 30' such as silicon oxide is blanket deposited over the surface of the created structure, patterned and etched to create contact openings 36'/37' over the source/drain regions and opening 38' over the top surface of the gate electrode. The metallization layer selectively deposited over the patterned dielectric establishes the electrical contacts 40'/42' with the source/drain regions and 44' with the top surface of the gate electrode.

5) page 18, third paragraph, please replace this paragraph with the following:

After the gate structure 14/16 has been formed LDD implants 18 are performed in order to reduce or eliminate the occurrence of leakage current between the gate electrode and the underlying silicon substrate. As typical LDD implant conditions can be cited an LDD implant for a NMOS device using arsenic with an energy within the range of between 1 to 10 keV and a dose within the range of between 1e14 to 1e16 atoms/cm^2. Also, an LDD implant for a PMOS implant using BF_2 with an energy within the range of between 1 to 10 keV and a dose within the range of between 1e14 to 5e15 atoms/cm^2.

6) page 21, third paragraph, please replace this paragraph with the following:

Next, Fig. 3, a silicon nitride liner 30 is deposited. The layer 30 of silicon nitride (Si_3N_4) can be deposited using LPCVD or PECVD procedures at a pressure between about 200 mTorr and 400 mTorr, at a temperature between about 600 and 800 degrees C., to a thickness of about 1500 to 3000 Angstrom using NH_3 and SiH_4 or $SiCl_2H_2$. The silicon nitride layer 30 can also be deposited using LPCVD or PECVD procedures using a reactant gas

mixture such as dichlorosilane ($SiCl_2H_2$) as a silicon source material and ammonia (NH_3) as a nitrogen source, at a temperature between about 600 and 800 degrees C., at a pressure between about 300 mTorr and 400 mTorr, to a thickness between about 200 and 300 Angstrom.

7) page 22, third paragraph, please replace this paragraph with the following:

The surface of layer 32 of BPSG is then polished using methods of CMP, down to the surface of layer 30 of silicon nitride, using the surface of layer 30 as the stop layer for the CMP process. This results in the cross section that is shown in Fig. 4.

8) page 22, last paragraph, page 23, first paragraph, please replace this paragraph with the following:

In the cross section that is shown in Fig. 4, it is clear that the surface of the layer 30 of silicon nitride is exposed where this layer overlays the gate electrode structure 14/16. This makes it possible to etch the layer 30 of silicon nitride over this exposed surface region and to remove the silicon

nitride of layer 30 from above the gate electrode structure 14/16.

9) page 48, please replace the ABSTRACT with the following new ABSTRACT:

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited. The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.